Research note

The influence of ferroelectric–electrode interface layer on the electrical characteristics of negative-capacitance ferroelectric double-gate field-effect transistors

Yongguang Xiao a, Minghua Tang a,*, Jiancheng Li b, Bo Jiang a, John He c

a Key Laboratory for Low Dimensional Materials and Application Technology of Ministry of Education (Xiangtan University), Xiangtan, Hunan 411105, China
b ASIC R&D Center, School of Electronic Science and Engineering of National University of Defense Technology, Changsha, Hunan 410073, China
c Pacific Geoscience Centre, Geological Survey of Canada, 9860 West Saanich Road, Sidney, British Columbia, Canada V8L 4B2

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The surface potential and subthreshold characteristics in negative capacitance (NC) double-gate ferroelectric field-effect transistor (FeFET) were investigated by considering the metal–ferroelectric interface layer. The derived results indicated that the negative capacitance regime which allows for amplified surface potential and steeper subthreshold characteristics were significantly affected by the interface layer. This imposes a severe limit to the step-up conversion capability and steeper subthreshold (<60 mV/dec) obtainable in the device. These results may provide some insight into the design and performance improvement for the low power dissipation FeFETs.

1. Introduction

In recent years, negative capacitance has been widely studied in both organic and inorganic semiconductor devices [1–10]. It is well-known that conventional field-effect transistors (FETs) require a change in the channel potential of at least 60 mV at room temperature to induce a change in the current by a factor of 10. This minimum subthreshold slope S puts a fundamental lower limit on the operating voltage and hence the power dissipation in standard FET-based switches. Recently, Salahuddin and Datta [9] suggested that the limit of 60 mV/dec can be reduced by replacing the conventional insulator in FETs with a ferroelectric insulator to form the so-called FeFETs. Salahuddin and Datta tried to exploit a negative capacitance regime of the ferroelectric in which the surface potential \(V_S\) of the semiconductor is up-converted and therefore the body factor of the transistor defined by \(m = \partial V_S / \partial V_g\), where \(V_g\) is the gate voltage, becomes smaller than one. Based on this idea, Jiménez et al. [10] proposed a physically-based analytical surface potential and drain current model and successfully optimized the performance of MFS-FET in terms of gain and \(V_S\) range by using properly engineered ferroelectric materials. However, the perfect contact between the metal gate electrodes and ferroelectric was tacitly assumed in their model. This is against the reality where an interface layer [11] or a dead layer [12] is usually sandwiched between the electrode and ferroelectric. Although the interface layer has been widely used to explain most of the abnormal behavior of ferroelectric [13–16] despite its poorly known nature and origin, not much attention has been paid to the interface layer effect on the electrical characteristics of NC-FeFETs. Since the up-converted surface potential could be used to enhance the electrostatic control of the gate electrode over the FET channel, it may open a new route toward steeper subthreshold transistors with \(S < 60 \text{ mV/dec} \) [10]. In this paper, the details of step-up conversion capability and subthreshold characteristics in the negative capacitance FeFETs were investigated by considering a thin non-switching interface layer (dead layer) between the ferroelectric and electrode.

2. Theoretical model

Based on Jiménez’s analytic model for surface potential and drain current [10], where a symmetric double gate (DG) NC-FET was investigated, we proposed an improved model with the ferroelectric–electrode interface layer by assuming the constant dielectric of 40. For simplicity and convenience, we assume that the two ferroelectric–electrode interface layers are symmetric and have the same physical characteristics as illustrated in Fig. 1. The total thickness of the interface layer and ferroelectric layer is denoted by \(t\). The thickness ratio \(\delta\) of the interface layer is defined as \(t_i / t\). In the following study, we take strontium bismuth tantalite (SBT) for the ferroelectric with a second-order phase transition. According to the Landau–Ginzburg–Devonshire’s (LGD) phenomenological [17], in the vicinity of a phase transition, the voltage across the ferroelectric can be expanded in powers of the charge with coefficients that can be experimentally determined.

* Corresponding author. Tel.: +86 731 58292200; fax: +86 731 58292468.
E-mail address: mhtang@xtu.edu.cn (M. Tang).

Generally, the electrostatic potential \( \phi(x) \) in the semiconductor can be written as [18]

\[
\phi(x) = V - \frac{2kT}{q} \ln \left( \frac{q^2n_i}{2\pi m^*_e kT} \cos \left( \frac{2\beta x}{t_s} \right) \right),
\]

where \( q \) is the electron charge, \( n_i \) is the intrinsic carrier concentration, \( \epsilon_r \) is the permittivity of the semiconductor, \( V \) is the electron quasi-Fermi potential, \( t_s \) is the thickness of the semiconductor layer, and \( \beta \) is a constant to be determined from the boundary condition that is given by

\[
V_g - V_d - \Delta \phi - \phi_s = a_0 + b_0 Q^3 + c_0 Q^2.
\]

where \( V_g \) is the voltage drop of the ferroelectric–electrode interface layer, \( \Delta \phi \) is the work function difference between the gate electrode and semiconductor. \( a_0, b_0, c_0 \) are constants dependent on the specific ferroelectric material. According to the boundary condition and electric displacement in MFS structure, \( V_g \) can be written as \( V_g = Q_{df}/\epsilon_{ef} \). Substituting it into Eq. (2), we can get

\[
V_g - \Delta \phi - \phi_s = (a_0 + t_s/\epsilon_{ef}) Q + b_0 Q^3 + c_0 Q^2.
\]

From Gauss’s law, the total mobile charge per unit gate area can be determined using \( Q = 2\epsilon_0 (d\phi(t_s/2)/dx) \) [19], which is equal to \((2C_s)(2kT/q)(2\beta) \tan(\beta)\). Where \( C_s = \epsilon_{ef}t_s \) is the structural capacitance. Substituting \( Q(\beta) \) into Eq. (3) leads to the following:

\[
(V_g - \Delta \phi - V) q = -\ln \left( \frac{2}{\epsilon_{ef} \sqrt{q^2 n_i}} \right) - \ln(\beta) - \ln[\cos(\beta)] + \left( a_0 + \frac{t_s}{\epsilon_{ef}} \right) 2C_s \beta \tan(\beta) + b_0 (2C_s) \beta \tan^3(\beta) + c_0 (2C_s) \beta \tan^5(\beta)
\]

\[
\times \tan^3(\beta),
\]

For a given \( V_g \), \( \beta \) can be solved from Eq. (4) as a function of \( V \). In order to obtain the drain current, the gradual channel approximation is assumed throughout this paper. Thus the current can be expressed as

\[
I_{ds} = \mu \frac{W}{L} \int_{0}^{\phi_s} Q(V) dV = \mu \frac{W}{L} \int_{\phi_s}^{\phi_g} Q(\beta) \frac{dV}{d\beta} d\beta.
\]

where \( \beta_L \) and \( \beta_R \) are the solutions of Eq. (4) corresponding to the cases of \( V = 0 \) and \( V = V_{ds} \), respectively. Substituting \( dV/d\beta \) (obtained from Eq. (4)) into Eq. (5) and performing the integration analytically yield to

\[
I_{ds} = \mu \frac{W}{L} \left[ \frac{4C_s W}{L} \left( \frac{2kT}{q} \right)^2 \left( \beta \tan(\beta) - \beta \right) + \left( a_0 + \frac{t_s}{\epsilon_{ef}} \right) C_s \beta^2 \tan^2(\beta) + 3b_0 (2C_s)^3 \left( \frac{2kT}{q} \right)^2 \beta^2 \tan^4(\beta)ight. + \left. \frac{5}{6} C_s (2C_s)^5 \left( \frac{4kT}{q} \right)^4 \beta^4 \tan^6(\beta) \right] \frac{dV}{d\beta}.
\]

Based on Eqs. (1)–(6), the characteristics of \( \phi_s - V_g, C_g - V_g, I_{ds} - V_g \) and \( I_{ds} - V_{ds} \) can be numerically obtained with the parameters used in [10].

3. Results and discussion

The calculated variations in \( \phi_s \) and \( V_g \) with different interface layer thickness at room temperature are shown in Fig. 2. The total thickness of the interface layer and the ferroelectric layer was assumed to be 20 nm. It can be seen that the step-up conversion capability of the MFS structure decreases remarkably when the interface layer becomes thicker. This can also be observed from the gain, which is defined as \( d\phi/dVg \) and shown in the inset of Fig. 2. Fig. 3 demonstrates the significant influence of the interface layer on the gate capacitance [20, 21]. The sharp peaks of the \( C_g - V_g \) curves are the indication of large gain, which become smaller with increasing the interface layer thickness as indicated in Fig. 3. The similar sharp peaks were also observed in previous study [22]. This may imply that the negative capacitance of ferroelectric is very likely presented in the structure, resulting in the relatively high value of \( C_g \). This can be explained by the series combination of a negative and a positive capacitor, in which the total capacitance surpasses that of its constituent positive capacitor. This is actually the opposite of what happens in a classical series combination of two positive capacitors where the total capacitance is always reduced. In fact, our result is comparable to the experimental report by Khan et al. [8].

It was previously suggested that the step-up conversion capability may be used as a mechanism to obtain steeper subthreshold transistor [10]. In order to investigate the interface layer effect on
the steeper subthreshold characteristics, we plotted the results of several cases with different interface layer thickness in Fig. 4a, assuming a uniform voltage drop ($V_{ds}$) of 0.01 V between the drain and source.

It can be seen clearly that the subthreshold swing $S$ appears to be a function of the interface layer thickness and it becomes bigger when the interface layer becomes thicker. This imposes a severe limit to the application of low power dissipation for the FeFET devices.

For a further view into the influence of interface layer on the electrical characteristics of FeFETs, the output characteristics with several different interface layer thicknesses was presented in Fig. 4b, where the gate voltage was kept at 0.8 V. It is observed that the ON-state current decreases when increasing the interface layer thickness ratio $\lambda$ which directly leads to the value deduction of $I_{ON}/I_{OFF}$. As a result, the difference between the ON state and the OFF state becomes small. The similar undesirable result for memory device was also reported in previous study [20].

It is worth to mention that from Eq. (6) we can see that enhancing the dielectric constant of ferroelectric–electrode interface layer could significantly improve the electrical characteristics of NC-MFS-FET such as the transfer and output characteristics. This suggests that the better control over the process of device arts and crafts and the improvement for the dielectric characteristics of the ferroelectric–electrode interface is of particularly important to the FeFET devices.

4. Conclusions

In summary, the effect of the ferroelectric–electrode interface on the electrical characteristics of NC-DG-FeFETs was examined. The derived results indicated that the step-up conversion capability, transfer and output characteristics were significantly affected by the ferroelectric–electrode interface layer. It can be concluded that the same result can be obtained when the dielectric interface layer exists between the ferroelectric film and semiconductor layer just as that pointed out by Jiménez et al. [10]. It was suggested that more attention should be paid to the arts and crafts of the devices.

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